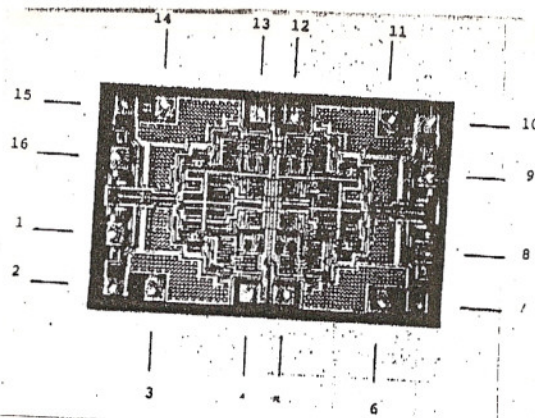




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



I/PAD FUNCTION:

IN 1	9. IN 3	25.
D1	10. D3	26.
S1	11. S3	27.
V-	12. VL	28.
. GND	13. V+(Substrate)	29.
. S4	14. S2	30.
7. D4	15. D2	31.
8. IN 4	16. IN 2	32.

Topside Metal: -
Backside: -
Backside Potential: -
Mask Ref: -
Bond Pads: .004"

APPROVED BY: CD
MFG: Siliconix

DIE SIZE: .070" x .109"
THICKNESS: -

DATE: 7/1/02
P/N: DG412A

DG 10.1.2
 Rev A 3-4-99